IN THE SPECIFICATION:

Please amend paragraph **[0008]** as follows:

[0008] The dielectric layer, in addition to physically protecting, sealing and isolating circuit traces on the substrate from contact with connective elements on the superimposed semiconductor die to prevent shorting, may be employed as desired as a structure to mechanically align the semiconductor die with the substrate for proper communication of the connective elements with the substrate terminals. This may be effected in the context of a so-called ~~"flip chip"~~ "flip-chip" semiconductor die bearing a pattern of discrete connective elements projecting transversely from the active surface of the die (such as solder bumps or conductive or conductor-bearing polymers), by using precisely sized and located apertures in the dielectric material to partially receive the connective elements. In addition to, or in lieu of, such an alignment structure approach, ~~upwardly projecting~~ upwardly projecting alignment elements comprising the same material as that of the dielectric layer may be fabricated on the dielectric layer. Such alignment elements may, for example, comprise C-shaped projections located on opposing sides of an intended location for the semiconductor die, L-shaped projections at corners of the intended die location, or linear segments parallel to, and defining a slightly larger area than, the side of a rectangular die.

Please amend paragraph **[0009]** as follows:

[0009] Such protective or alignment elements may be applied to a dielectric layer or layer segments using stereolithographic techniques. Formation of the protective or alignment structures is accomplished by suspending a substrate on a support platform within a reservoir containing a curable liquid as commonly used in stereolithography (typically a photopolymer). The platform is vertically moveable such that a substrate suspended thereon may be moved in precise increments into or out of the curable liquid. Layer thickness and shape for the desired stereolithographic formations are typically ~~programed~~ programmed into a computer control system which monitors the stereolithographic process. In response to the control system, the platform upon which a substrate is suspended is lowered into the reservoir to a desired depth within the liquid such that a layer of curable liquid in the reservoir covers or lies adjacent a

certain level with respect to the suspended substrate. Precisely focused electromagnetic radiation in the form of an ultraviolet (UV) wavelength laser is triggered to fix or cure at least a portion of the liquid material on or adjacent the substrate. The platform is then lowered by a distance equal to the thickness of the next desired layer to provide a new layer of curable liquid and the laser is again triggered to cure at least a portion of the liquid. The process is then repeated layer by layer until the desired stereolithographic structure is formed on and about the substrate. The platform is then raised above the level of the liquid and the substrate with associated stereolithographic structure is removed.

Please amend paragraph **[0011]** as follows:

[0011] By their diminutive nature in terms of gross dimensions and the minute features and elements thereof, semiconductor dice and other components such as test interposers, leads and other connective elements, interposers for converting dice to a ~~flip chip~~ flip-chip configuration and other, similar structures (hereinafter generally and collectively termed "electronic components") are very fragile and susceptible to damage in addition to lacking structural rigidity, including torsional rigidity. This is particularly true of bare (unpackaged) semiconductor dice. Thus, exposure of semiconductor dice and other minute components to the processing and handling steps involved in stereolithographic methods can result in damage to or destruction of the components.

Please amend paragraph **[0015]** as follows:

[0015] It has been disclosed and claimed in U.S. patent application Serial ~~No.09/259,142,~~ No. 09/259,142, assigned to the assignee of the present invention and issued as U.S. Patent No. 6,549,821, to modify a conventional stereolithography apparatus such as those offered by 3D Systems, Inc. with a machine vision system to precisely locate features on electronic components so as to enable fabrication of stereolithographic structures thereon. While a machine vision system enables fabrication of such structures on a large plurality of electronic components residing on a platform of a stereolithography apparatus and while a machine vision system may be employed to plot the gross (general) location and orientation of electronic

components on a platform, such an approach may undesirably consume computer processing power as well as require a machine vision system employing two camera systems, one for determining the gross locations and orientations of the electronic components and another one for focusing on the surfaces, elements and features of an individual electronic component for precise placement of stereolithographic structures thereon. In addition, such an approach still requires handling of individual electronic components or electronic component assemblies to place same on the platform for fabrication of the stereolithographic structures and remove same after fabrication thereof for further processing. This necessity both enhances the potential for damage and contamination and inhibits automation of the stereolithography process for the described applications.

Please amend paragraph **[0023]** as follows:

[0023] Another embodiment of the present invention encompasses the gross location and orientation of a plurality of individual electronic components by adhering them in position to a UV-radiation sensitive adhesive-coated film such as is employed in singulation of semiconductor dice from a wafer or other large-scale semiconductor substrate. In this embodiment, individual electronic components in the form of, for example, semiconductor dice may be placed and adhered in preselected, mutually laterally spaced locations in desired orientations to the film, which is supported by a frame member having alignment features thereon configured for engagement with alignment elements on a stereolithography platform or the like. The semiconductor dice may then have stereolithographic structures such as packaging envelopes formed on as many as five sides thereof, the sixth downward-facing side being adhered to the adhesive-coated film. Since silicon is opaque to UV radiation, use of a UV wavelength laser beam to cure the curable liquid into at least a semisolid structure will not release the semiconductor dice from the film. Thus, after the stereolithographic structures have been formed, the frame member bearing the film and now substantially encapsulated semiconductor dice thereon may be removed from the curable liquid in the reservoir, the excess liquid drained off and cleaned as desired. The frame may then be placed in an oven to accelerate and complete curing of the packaging envelopes, after which the frame may be inverted, the

underside (now top side) of the inverted film exposed to broad source UV wavelength radiation to alter the characteristics of the UV radiation-sensitive adhesive, and the semiconductor dice released into, for example, a tray having cells sized and configured to receive each substantially packaged (five sides thereof) semiconductor die. Alternatively, the semiconductor dice may be released onto another adhesive-coated film. If the now upwardly facing, bare sixth side of each semiconductor die comprises an active surface bearing bond pads or trace ends for rerouting bond pads for external connection to higher level packaging, the bond pads or trace ends may have discrete conductive elements formed or placed thereon to complete a so-called ~~"flip chip"~~ "flip-chip" die as known in the art. It is contemplated that the discrete conductive elements may comprise solder balls or other metal or alloy balls or bumps, conductive epoxy bumps or pillars, or conductor-filled epoxy bumps or pillars, all as known in the art. The locational and orientational fixation provided by the tray cells facilitates the formation or placement of the discrete conductive elements.

Please amend paragraph **[0032]** as follows:

[0032] FIG. 6 is a side elevation of the embodiment of ~~FIG. 6;~~ FIG. 5;

Please amend paragraph **[0038]** as follows:

[0038] Apparatus 10 also includes a reservoir 14 (which may comprise a removable reservoir interchangeable with others containing different materials) of liquid material 16 to be employed in fabricating the intended object. In the currently preferred embodiment, the liquid is a photo-curable polymer (hereinafter "photopolymer") responsive to light in the UV wavelength range. The surface level 18 of the liquid material 16 is automatically maintained at an extremely precise, constant magnitude by devices known in the art responsive to output of sensors within apparatus 10 and preferably under control of computer 12. A support platform or elevator 20, precisely vertically movable in fine, repeatable increments responsive to control of computer 12, is located for movement downward into and upward out of liquid material 16 in reservoir 14. A UV wavelength range laser plus associated optics and galvanometers (collectively identified as 22) for controlling the scan of laser beam 26 in the X-Y plane across platform 20 has

associated therewith mirror 24 to reflect beam 26 downwardly as beam 28 toward surface 30 of platform 20. Beam 28 is traversed in a selected pattern in the X-Y plane, that is to say, in a plane parallel to surface 30, by initiation of the galvanometers under control of computer 12 to at least partially cure, by impingement thereon, selected portions of liquid material 16 disposed over surface 30 to at least a semisolid state. The use of mirror 24 lengthens the path of the laser ~~beam,~~ beam 26, effectively doubling same, and provides a more vertical beam 28 than would be possible if the laser 22 itself were mounted directly above platform surface 30, thus enhancing resolution.

Please amend paragraph **[0041]** as follows:

[0041] Before initiation of a first layer for a base support 52 or object 50 is commenced, computer 12 automatically checks and, if necessary, adjusts by means known in the art, the surface level 18 of liquid material 16 in reservoir 14 to maintain same at an appropriate focal length for laser beam 28. U.S. Patent 5,174,931, referenced above and previously incorporated herein by reference, discloses one suitable level control system. Alternatively, the height of mirror 24 may be adjusted responsive to a detected surface level 18 to cause the focal point of laser beam 28 to be located precisely at the surface of liquid material 16 at surface level 18 if level 18 is permitted to vary, although this approach is somewhat more complex. The platform 20 may then be submerged in liquid material 16 in reservoir 14 to a depth equal to the thickness of one layer or slice of the object 50, and the liquid surface level 18 readjusted as required to accommodate liquid material 16 displaced by submergence of platform 20. Laser 22 is then activated so that laser beam 28 will scan liquid material 16 over surface 30 of platform 20 to at least partially cure (e.g., at least partially polymerize) liquid material 16 at selective locations, defining the boundaries of a first layer 60 (of object 50 or base support 52, as the case may be) and filling in solid portions thereof. Platform 20 is then lowered by a distance equal to the thickness of a layer 60, and the laser beam 28 scanned to define and fill in the second layer 60 while simultaneously bonding the second layer to the first. The process is then repeated, layer by layer, until object 50 is completed.

Please amend paragraph **[0046]** as follows:

[0046] Each layer 60 of object 50 is preferably built by first defining any internal and external object boundaries of that layer with laser beam 28, then hatching solid areas of object 50 with laser beam 28. If a particular part of a particular layer 60 is to form a boundary of a void in the object above or below that layer 60, then the laser beam 28 is scanned in a series of ~~closely spaced,~~ closely spaced, parallel vectors so as to develop a continuous surface, or skin, with improved strength and resolution. The time it takes to form each layer 60 depends upon its geometry, surface tension and viscosity of liquid material 16, and thickness of the layer.

Please amend paragraph **[0048]** as follows:

[0048] In practicing the present invention, a commercially available stereolithography apparatus operating generally in the manner as that described with respect to apparatus 10 of FIG. 1 is currently preferably employed. For example and not by way of limitation, the SLA-250/50HR, SLA-5000 and SLA-7000 stereolithography systems, each offered by 3D Systems, Inc., of Valencia, California are suitable for practice of the present invention. Photopolymers believed to be suitable for use in practicing the present invention include Cibatool SL 5170 and SL 5210 resins for the SLA-250/50HR system, Cibatool SL 5530 resin for the SLA-5000 system and Cibatool SL 7510 resin for the SLA-7000 system. All of these resins are available from Ciba Specialty Chemicals ~~Corporation.~~ Inc. By way of example and not limitation, the layer thickness of liquid material 16 to be formed, for purposes of the invention, may be on the order of 0.001 to 0.020 inch, with a high degree of uniformity over a field ~~on a~~ on surface 30 ~~of a~~ of platform 20. It should be noted that different material layers may be of different heights, so as to form a structure of a precise, intended total height or to provide different material thicknesses for different portions of a structure. The size of the laser beam ~~"spot"~~ "spot" 76 impinging on the surface of liquid material 16 to cure same may be on the order of 0.002 inch to 0.008 inch. Resolution is preferably ± 0.0003 inch in the X-Y plane (parallel to surface 30) over at least a 0.5 inch X .25 inch field from a center point, permitting a high resolution scan effectively across a 1.0 inch X 0.5 inch area. Of course, it is desirable to have substantially this high a resolution across the entirety of surface 30 of platform 20 to be scanned

by laser beam 28, which area may be termed the "field of ~~exposure",~~ exposure," such area being substantially coextensive with the vision field of a machine vision system employed in the apparatus of the invention as explained in more detail below. The longer and more effectively vertical the path of laser beam 26/28, the greater the achievable resolution.

Please amend paragraph **[0049]** as follows:

[0049] Referring again to FIG. 1 of the drawings, it should be noted that apparatus 10 of the present invention includes a camera 70 which is in communication with computer 12 and preferably located, as shown, in close proximity to mirror 24 located above surface 30 of platform 20. Camera 70 may be any one of a number of commercially available cameras, such as capacitive-coupled discharge (CCD) cameras available from a number of vendors. Suitable circuitry as required for adapting the output of camera 70 for use by computer 12 may be incorporated in a board 72 installed in computer 12, which is programmed as known in the art to respond to images generated by camera 70 and processed by board 72. Camera 70 and board 72 may together comprise a so-called "machine vision ~~system",~~ system," and specifically a "pattern recognition system" (PRS), the operation of which will be described briefly below for a better understanding of the present invention. It should also be noted that the thickness of liquid material 16 forming a layer 60 over a selected portion of a given object 50 may be altered object by object, again responsive to output of camera 70 or one or more additional cameras ~~74, 76~~ 74 or 78, shown in broken lines, detecting a protrusion or height of elements or features which should be, but are not, covered by the "design" or preprogrammed thickness of liquid material 16 disposed over and at least partially cured on a prior layer 60. Such capability is particularly useful when creating objects 50 in the form of stereolithographic structures adjacent or over preformed components on or over platform 20, such as is involved in practice of the present invention. Alternatively, a self-contained machine vision system available from a commercial vendor of such equipment may be employed. For example, and without limitation, such systems are available from Cognex Corporation of Natick, Massachusetts. For example, the apparatus of the Cognex BGA Inspection Package™ or the SMD Placement Guidance Package™ may be adapted to the present invention, although it is believed that the MVS-8000™ product family and

the Checkpoint® product line, the latter employed in combination with Cognex PatMax™ software, may be especially suitable for use in the present invention.

Please amend paragraph **[0052]** as follows:

[0052] Upper platen 120 is shown in partial section in FIG. 3 above lower platen 102 bearing multi-chip modules 200 to better depict component assembly cavities 122 in upper platen 120, the side walls 124 of which frame the locations of semiconductor dice 206 on ~~printed circuit boards~~ carrier substrates 204, for example, printed circuit boards. Platen alignment element receptacles in the form of pin receptacles 126 in upper platen 120 are shown in alignment with pins 104 of lower platen 102, with exaggerated clearances therebetween for clarity of illustration, so when upper platen 120 is lowered onto lower platen 102, pins 104 will also align upper platen 120, and consequently component assembly cavities 122, over semiconductor dice 206. As shown in broken lines in FIG. 3, component assembly cavities 122 may be subdivided by compression struts 127 into subcavities 122a, each of which is sized and located to receive a single semiconductor die 206. When upper platen 120 is lowered completely over lower platen 102 in alignment therewith and with multi-chip modules 200 trapped therebetween, upper platen 120 and lower platen 102 may be secured together to clamp ~~printed circuit boards~~ carrier substrates 204 in a completely planar configuration, substantially eliminating any potential for board warping or twisting. The use of compression struts 127 further ensures the planarity of ~~printed circuit boards~~ carrier substrates 204 by providing multiple points of contact and loading by upper platen 120 oriented Normal to the plane of ~~printed circuit board~~ carrier substrates 204 to preclude bowing of ~~printed circuit boards~~ carrier substrates 204. Upper platen 120 may be releasably secured to lower platen 102 by any suitable structure including, for example, clamps 130 engaging aligned flanges 132 on opposing edges of upper and lower platens 120, 102 as illustrated, spring clips, bolts or other means known in the art.

Please amend paragraph **[0053]** as follows:

[0053] It will be appreciated by those of ordinary skill in the art that component assembly cavities 122 and subcavities 122a are sized and configured with enough lateral clearance between semiconductor dice 206 and side walls 124, including the side walls of compression struts 127, for formation of stereolithographic structures adjacent semiconductor dice 206 without the potential for curing liquid solidifying in adherence to the side walls 124. Of course, if the semiconductor dice 206 are wire bonded to traces on the ~~printed circuit board~~ carrier substrate 204 as shown with respect to left-most semiconductor die 206a in FIG. 3, the lateral clearance will be sufficient to avoid the laterally outer ends of the bond wires 208 bonded between bond pads 210 on semiconductor die 206a and the ends of circuit traces 212 on printed circuit board 204a so as to prevent damage to the bond wires 208 and permit the bond wires 208 to be stereolithographically enveloped by curing of the curable liquid. On the other hand, if a semiconductor die 206 of multi-chip module 200 is a flip-chip die such as right-most semiconductor die 206b in FIG. 3, lateral clearance may be reduced, as discrete conductive elements 214 provide mechanical and electrical connections between semiconductor die 206b and circuit traces 212 on printed circuit board 204b. As noted previously, curable liquid trapped between semiconductor die 206b and printed circuit board 204b may be cured by postcuring in, for example, an oven due to heat-initiated cross linking of the trapped curable liquid, providing an underfill between semiconductor die 206b and printed circuit board 204b, the heat also accelerating the complete cure of other portions of the stereolithographically applied dielectric material. A suitable temperature for postcuring is about 120°C.

Please amend paragraph **[0054]** as follows:

[0054] As further depicted in FIG. 3, lower platen 102 is desirably provided with platen assembly alignment features such as, for example, apertures 140 for engagement with platen assembly alignment elements 150 projecting from platform 20 as previously identified with respect to FIG. 1 (clearances between platen assembly alignment elements 150 and interiors of apertures 140 being exaggerated for clarity), these cooperative structures ensuring a desired placement of double platen assembly 100 on platform 20 and thus of multi-chip modules 200

secured to double platen assembly 100. The double platen assembly 100 carrying multi-chip modules 200 is incrementally submerged in the curable liquid material 16 within a reservoir 14 and a stereolithographic package structure comprising a plurality of layers of at least partially cured liquid material 16 fabricated as previously described. In the case of active surface-up semiconductor dice 206, it is contemplated that four (4) sides of each die would be encapsulated and the active surface covered except for bond pad locations, unless bond wires 208 extending to circuit traces 212 on ~~printed circuit board~~ carrier substrate 204 have already been formed, in which instance bond wires 208 and the underlying bond pads 210 would also be covered. In the case of active surface-down semiconductor dice 206, it is contemplated that five (5) sides of each die would be encapsulated, the sixth, downward-facing active surface remaining free of packaging material.

Please amend paragraph **[0055]** as follows:

[0055] After all semiconductor dice 206 of multi-chip modules 200 have had stereolithographic structures formed thereon, double platen assembly 100 is raised above the level of liquid material 16 and lower platen 102 disengaged from alignment elements 150 of platform 20. Excess liquid material 16 may be drained from double platen assembly 100 back into reservoir 14, then double platen assembly 100 with at least partially packaged semiconductor dice 206 may be removed from apparatus 10 with their ~~printed circuit boards~~ carrier substrates 204 and cleaned, if desired.

Please amend paragraph **[0056]** as follows:

[0056] As depicted in FIG. 4, the double platen assembly of the present invention may be fabricated as an embodiment 100′ adapted to multi-component assemblies 300 using carrier substrates in the form of lead frame strips 304 having semiconductor dice 206 secured thereto. As shown, semiconductor dice 206 are configured with central rows of bond pads (not shown) wire bonded ~~at~~ with bond wires 208 to leads 306 of lead frames of lead frame strips 304 and are adhered by their active surfaces to the undersides of leads 306 of lead frames of lead frame strips 304 in a ~~leads over chip,~~ leads-over-chip, or LOC, configuration as known in the art.

Thus, lower platen 102′ is provided with component assembly cavities 122′ (including, as desired, subcavities 122′a) to receive the semiconductor dice 206 suspended from lead frame strips 304. In this embodiment, pins 104 are sized and located to project through selected apertures 302 in the form of indexing holes conventionally employed in lead frame strips 304. Upper platen 120′ includes the same features as previously described with respect to upper platen 120, with component assembly cavities 122 and subcavities 122a (again, as desired) sized and configured with appropriate lateral clearances about semiconductor dice 206. With embodiment 100′, the double platen assembly may be placed on and engaged with a platform 20 of a stereolithography apparatus, stereolithographic packaging structures formed as described previously on semiconductor dice 206 including encapsulation of bond wires 208, double platen assembly 100′ removed from the stereolithography apparatus, inverted and reengaged with platform 20 by a second set of platen assembly alignment ~~aperatures~~ apertures 140 with platen assembly alignment elements 150 (not shown in FIG. 4), and the backside and lateral sides of semiconductor dice 206 encapsulated with a dielectric, stereolithographically formed structure to complete packaging thereof, cavities 122′ and subcavities 122′a providing access to semiconductor dice 206 with double platen assembly 100′ in an inverted orientation. It is also contemplated that a suitably configured double platen assembly 100′ may be used to encapsulate semiconductor dice 206 on two opposing sides of a multi-chip module 200, modules so configured being well known in the art.

Please amend paragraph **[0057]** as follows:

[0057] In lieu of removing a double platen assembly 100′ from a stereolithography apparatus in order to invert the double platen assembly 100′, stereolithography apparatus 10 may be configured with a platen assembly support structure 400 as schematically depicted in FIG. 7 of the drawings. Platen assembly support structure 400 may include opposing towers 402, each having a platen assembly engagement structure 404 for engaging a double platen assembly 100′ from opposing sides thereof, the platen assembly engagement structures 404 being rotatable about mutually aligned horizontal axes A. Bearing assemblies (not shown) may be employed to facilitate smooth rotation and a high degree of precision of alignment of horizontal axes A so that

double platen assembly 100′ and all features thereof as well as the positions of multi-chip modules 200 or multi-component assemblies 300 will not be shifted in position in the X-Y plane and will thereby be easily recognizable and locatable by camera 70 of the machine vision system of apparatus 10. These coincident axes A permit 180° inversion of a double platen assembly 100′ to facilitate formation of stereolithographic structures on electronic components on both sides of a carrier substrate such as ~~a printed circuit board~~ carrier substrate 204 or exposed from both sides of a carrier substrate such as a lead frame strip 304. The double platen assembly 100′ may be locked in either an upright or inverted position by any suitable device known in the art with the carrier substrate 204, 304 on a level plane. Inversion of double platen assembly 100′ may be automated using a rotary stepper motor or other suitable motor 406. Initiation of rotation and termination thereof may be automated and under the control of computer 12 of apparatus 10. Thus, stereolithographic structures may be formed adjacent to semiconductor dice 206 on both sides of ~~a printed circuit board~~ carrier substrate 204 or adjacent all sides of semiconductor dice carried by a lead frame strip 304 without removal of double platen assembly 100′ from stereolithography apparatus 10.

Please amend paragraph **[0059]** as follows:

[0059] In a method of the present invention employing the apparatus of FIGS. 3 and 4, a lower platen 102, 102′ of a double platen assembly 100, 100′ is loaded with multi-chip modules 200 as described above, the upper platen 120, 120′ superimposed thereon and secured thereto, and the loaded double platen assembly 100, 100′ placed on a platform 20 of a stereolithography apparatus 10 with the alignment ~~aperatures~~ apertures 140 of the lower platen 102 engaged with alignment elements 150 of platform 20. The double platen assembly ~~200~~ 100, 100′ is incrementally submerged in the curable liquid material 16 within a reservoir 14 and a stereolithographic package structure comprising a plurality of layers of at least partially cured liquid material 16 fabricated on each semiconductor die 206 as previously described. In the case of active surface-up semiconductor dice 206, it is contemplated that four sides of each die would be encapsulated, and the active surface covered except for bond pad locations. In the case of active surface-down semiconductor dice 206, it is contemplated that all six sides of each

semiconductor die 206 would be encapsulated, the sixth, downward-facing active surface being encapsulated about discrete conductive elements 214 due to cross linking of liquid material 16 trapped between the dice 206 and the ~~printed circuit boards~~ carrier substrates 204 in association with the cross linking of the surrounding sides of the stereolithographic structure having cross linking directly initiated by exposure to the UV laser beam.

Please amend paragraph **[0061]** as follows:

[0061] In a method of the present invention employing double platen assembly 100′, the acts are the same except that double platen assembly 100′ is inverted and reengaged with alignment elements 150 of platform 20 and the remaining, unencapsulated portions of semiconductor dice 206 ~~stereolithgraphically~~ stereolithographically encapsulated, as desired. The double platen assembly 100′ is then raised out of liquid material 16, drained, cleaned and multi-component assemblies 300 in the form of lead frame strips 304 bearing semiconductor dice 206 removed from double platen assembly 100′. As noted previously, this method may also be used with multi-chip modules 200 bearing semiconductor dice 206 on opposing sides thereof.

Please amend paragraph **[0062]** as follows:

[0062] Referring now to FIGS. 5 and 6 of the drawings, a further embodiment of the present invention comprising frame assembly 500 includes a frame member 502 having suspended therein under tension a film 504 having an ultraviolet (UV) wavelength-sensitive adhesive 506 disposed on an upper surface. As shown, frame member 502 may be a two-part frame comprising parts 502a and 502b, and film 504 is placed under tension by stretching it over one part 502a and then clamping the other part 502b to the one part 502a to maintain the film tension. Suitable UV radiation-sensitive adhesive-coated films are available from 3M and Nitto Denko, the film selected being at least somewhat a function of the temperature to which it may be exposed during processing. For example, 3M offers a film which does not degrade until reaching about 320°C, while Nitto Denko film degrades at a far lower temperature (140°C), but is far less costly. Frame member 502 includes alignment features such as, for example, apertures 140 for engagement with alignment ~~elements~~ elements 150 projecting from

platform 20 as previously identified with respect to ~~FIG. 1,~~ FIG. 3, these cooperative structures ensuring a desired placement of frame member 502 on platform 20 and thus of semiconductor dice 206 adhered to film 504.

Please amend paragraph **[0063]** as follows:

[0063] In practice, a ~~pick and place~~ pick-and-place machine as known in the art may be employed to remove electronic components such as semiconductor dice 206 from, for example, a so-called JEDEC tray having a plurality of cells therein arranged in rows and columns (only some semiconductor dice 206 shown by way of example in FIG. 5), each cell containing a single semiconductor die 206, and place each removed semiconductor die on film 504 at a preprogrammed location within a resolution of about ± one to two mils, or one to two thousandths of an inch, such ~~pick and place~~ pick-and-place equipment being commercially available. Thus, a plurality of semiconductor dice 206 may be placed in an array of, for example, rows and columns and mutually laterally spaced with a lateral clearance (also termed "spacing or pitch") between individual semiconductor dice 206 sufficient to form stereolithographic structures thereabout. The semiconductor dice 206 may be placed active surface up and configured with bond pads or rerouted bond pads 210 positioned for wire bonding, or may be placed active surface down in the case of semiconductor dice to be configured as ~~flip chips,~~ flip-chips, with discrete conductive elements such as solder balls to be placed or formed on an array of bond pads or rerouted bond pads 210. Both configurations of semiconductor dice 206 are depicted in FIGS. 5 and 6 for clarity.

Please amend paragraph **[0064]** as follows:

[0064] In a method of the present invention employing the apparatus of FIGS. 5 and 6, a frame assembly 500 having semiconductor dice 206 disposed on film 504 and adhered to adhesive 506 is secured by alignment features, for example, alignment apertures 140 to the alignment elements 150 of a platform 20 of a stereolithography apparatus 10. The frame assembly 500 is incrementally submerged in the curable liquid material 16 within a reservoir 14 and a stereolithographic package structure comprising a plurality of layers of at least partially

cured liquid material 16 fabricated on each semiconductor die 206 as previously described. In the case of active surface-up semiconductor dice 206, it is contemplated that four sides of each die would be encapsulated, and the active surface covered except for bond pad locations. In the case of active surface-down semiconductor dice 206, it is contemplated that five (5) sides of each die would be encapsulated, the sixth, downward-facing active surface remaining free of packaging material.

Please amend paragraph **[0065]** as follows:

[0065] After all semiconductor dice 206 on film 504 have had stereolithographic structures formed thereon, frame assembly 500 is raised above the level of liquid material 16 and frame member 502 disengaged from alignment elements 150 of platform 20. Excess liquid material 16 may be drained from frame assembly 500 back into reservoir 14, then frame ~~assembly~~ assembly 500 with at least partially packaged semiconductor dice 206 adhered thereto removed from apparatus 10 and cleaned, if desired. Frame assembly 500 may then be placed in an oven to accelerate and complete the cure of the stereolithographic packaging structures, or subjected to broad source UV radiation for the same purpose. Subsequently, frame assembly 500 is inverted over, for example, a tray such as another JEDEC tray or other suitable receptacle and subjected to broad source UV radiation from above to cause adhesive 506 to release semiconductor dice 206 from film 504. It should be noted again that the UV laser beam and optional broad source UV radiation do not degrade adhesive 506 when frame assembly 500 is right-side up, as silicon is opaque to UV radiation and so the adhesive 506 underlying each semiconductor die 206 is not exposed. Instead of releasing semiconductor dice 206 into a JEDEC tray or other receptacle, it is contemplated that semiconductor dice 206 may be released onto another frame assembly 500 and adhered to a film 504 thereof by a UV radiation-sensitive adhesive 506 for further processing in stereolithography apparatus 10 or elsewhere.

Please amend paragraph **[0066]** as follows:

[0066] After semiconductor dice 206 are released from film 504, they may then be processed further. For example, in the case of the semiconductor dice 206 encapsulated on four

sides and over the active surface, but for the bond pad locations, these may then be picked up by another ~~pick and place~~ pick-and-place machine and secured to die sites on a carrier substrate to form a multi-chip module and then wire bonded or otherwise electrically connected, as by TAB elements comprising circuit traces on a flexible dielectric film, to circuit traces on the carrier substrate. In the case of the semiconductor dice 206 encapsulated on five sides, the semiconductor dice 206 may be released into a receptacle having a plurality of rectangular cells therein to maintain alignment of the semiconductor dice 206 in an array and reinserted into an apparatus 10 where the now upward-facing sixth side (active surface) may be encapsulated, but for the bond pad locations. Alternatively, as noted above, the semiconductor dice 206 may be released onto film 504 of another frame assembly 500. After this operation is complete, the packages are completely cured and the semiconductor dice 206 are cleaned, and discrete conductive elements such as solder balls, conductive epoxy bumps or pillars or conductor-filled epoxy bumps or pillars are placed or formed on the bond pads 210 to complete the fabrication of flip-chip semiconductor dice 206. It should also be noted that, instead of bare semiconductor dice 206, semiconductor dice 206 secured and electrically connected to conductively bumped interposers may be placed with bumps down and adhered to film 504, and the exposed sides and backside of each semiconductor die 206 encapsulated to complete packaging thereof. Further, either before or after five-sided stereolithographic packaging structures are formed, a Z-axis anisotropically conductive film as known in the art may be adhered to the active surfaces and thus over the bond pads 210 of semiconductor dice 206 in lieu of discrete conductive elements to provide external electrical connections for each semiconductor die 206.

Please amend paragraph **[0067]** as follows:

[0067] As a further variation of the invention, and with reference to FIG. 8 of the drawings, a tray or film (film 504 shown) carrying active surface-up semiconductor dice 206 may be placed in a stereolithography apparatus 10, the active surface sides ~~thereof 207~~ 207 thereof covered with cured dielectric material 600 but for apertures 602 exposing bond pads or trace ends 604. Discrete conductive elements 608 as shown with respect to center semiconductor die 206 may then be formed or placed in the apertures 602 in contact with bond pads or trace

ends 604 after the tray or film has been removed from the stereolithography ~~apparatus,~~ apparatus 10, any excess curable liquid removed, the semiconductor dice 206 cleaned to remove excess curable liquid from the apertures 602 and the dielectric material 600 covering the active surface sides 207 further cured as necessary or desired. Discrete conductive elements 608 may comprise, for example, solder or other metal or alloy balls or bumps, or a conductive or conductor-filled epoxy, as known in the art. The discrete conductive elements 608 may be preformed or formed in place on semiconductor dice 206. Of course, the side walls 206s of semiconductor dice 206 may also be encapsulated concurrently with the active surface sides 207 as described previously and as shown in broken lines in FIG. 8.